CLAIMS

1. Digital signal processing system comprising a processor exploiting n-bit words provided by an analog-to-digital converter, characterized in that the analog-to-digital converter is adapted to provide (n+m) bit samples and in that the system comprises selection means for providing the processor with the n least significant bit of the sample is within the n least significant bits, and with n consecutive bits up to the first non-zero most significant bit when said first non-zero most significant bit is among the m most significant bits, the processor being adapted to multiply each n-bit word thus received by a factor corresponding to the offset of the n-bit word with respect to the n least significant bits.

2. Digital signal processing system according to claim 1, characterized in that the processor has a bus having a width at least equal to n+m, wherein the output of the analog-to-digital converter is aligned with the least significant bits of said bus and said selection means is adapted to cancel the least significant bits of the bus which are not within said n-bit word.

3. Digital signal processing system according to claim 1, characterized in that the analog-to-digital converter is constructed to have an n-bit accuracy.